# EXPERIMENT 3--INTRODUCTION TO COMBINATIONAL LOGIC AND BUS STRUCTURE

# FINAL REPORT

**I. *Function***

a). Draw the logic diagram for your circuit of part A.1. Indicate on the diagram the longest propagation path through the circuit. Also, give the logic levels on all the lines in the circuit, other than on this path, for an input combination that sensitizes this path. (The path is sensitized if a change on the path input propagates all the way to the output.)

b). Include the Karnaugh Map function expressions from Part 1 of the Prelab.

c). Either sketch or include the captured waveforms observed on the scope in determining the longest propagation delay of the circuit in Part A.



**LOW to HIGH Output Transition**



**HIGH to LOW Output Transition**

d). From your scope waveforms determine the average propagation delay through the longest path of the circuit in part A.

**II. *Cascading***

a). Include your waveform diagram showing the longest propagation time between Ci and Co in the cascade circuit. For this situation, if S1 and S0 are constant, describe in words the function performed by the cascade circuit?

b). If 16 copies of the circuit were cascaded in the same manner, what would be the maximum propagation delay through the circuit?

**III. *Bus Structure***

a). Designate the value on the tri-state bus as OUT. Fill in the table combinations below and derive the switching algebra expression for OUT.

Enable A B OUT

0 0 0

0 0 1

0 1 0

0 1 1

1 0 0

1 0 1

1 1 0

1 1 1

b) Sketch output waveforms observed on the scope from part C.2.



**LOW to HIGH Output Transition**



**HIGH to LOW Output Transition**

c) How could the circuit of Figure 4.6 be modified so that the bus could be placed in a high-impedance state when desired? Draw a circuit diagram for the new design and explain its operation.